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EXAMINER
VIGUSHIN, JOHN B

ART UNIT	PAPER NUMBER
2827	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/911,760	Applicant(s) MCCALL ET AL.
	Examiner John B. Vigushin	Art Unit 2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 July 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *23 and 24* is/are allowed.

6)☒ Claim(s) *1-5,7,8,12,13,15-22 and 25-29* is/are rejected.

7)☒ Claim(s) *6,9-11 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claims 10, 11 and 14 are objected to because of the following informalities:

In Claim 10, line 6: --second-- should be inserted before "section".

In Claim 11, line 6: --second-- should be inserted before "section".

In Claim 11, line 6: "a" (occurring after "for") should be deleted.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 17 and 19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 17 and 19 each recite the limitation "on the path" in line 2. There is insufficient antecedent basis for this limitation in the claim. Which "path" is contemplated: the first data path, the second data path, some other path? Furthermore, Claims 17 and 19 both recite identical subject matter and both depend from base Claim 20, so it appears that one of Claims 17 and 19 should be cancelled.

Double Patenting

4. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or

discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

5. Claims 21, 22, 25, 26 and 29 are provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of Claims 25-29, respectively, of copending Application No. 09/911,635, filed July 23, 2001. This is a provisional double patenting rejection since the conflicting claims have not in fact been patented.

6. Claims 21, 22, 25, 26 and 29 are directed to the same invention as that of Claims 25-29, respectively, of commonly assigned Application No. 09/911,635. The issue of priority under 35 U.S.C. 102(g) and possibly 35 U.S.C. 102(f) of this single invention must be resolved.

Since the U.S. Patent and Trademark Office normally will not institute an interference between applications or a patent and an application of common ownership (see MPEP § 2302), the assignee is required to state which entity is the prior inventor of the conflicting subject matter. A terminal disclaimer has no effect in this situation since the basis for refusing more than one patent is priority of invention under 35 U.S.C. 102(f) or (g) and not an extension of monopoly.

Failure to comply with this requirement will result in a holding of abandonment of this application.

7. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

8. Claims 27 and 28 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 25 of copending Application No. 09/911,635. Although the conflicting claims are not identical, they are not patentably distinct from each other as shown in the following explanation:

Claim 25 of Appln. No. 09/911,635 recites all the limitations of Claim 27 of the instant Application but does not teach a buffer on each of the first and second modules; also, Claim 25 of Appln. No. 09/911,635 recites all the limitations of Claim 28 of the instant Application but does not teach error correction code chips on each of the first and second modules. However, buffers and error correction code chips are old and well-known devices for performing specific functions in an electronic circuit when mounted on a multichip modular or system circuit board, such as a circuit board typically having memory devices, processors and/or controllers mounted thereon in a computer environment. Buffers have various electronic circuit functions: *inter alia*, as storage sites that temporarily store data during transfers to compensate for differences in data

flow rates. Error correction code (ECC) chips are typically used for generating correction code when data is written into a memory chip and for checking "read" data to correct errors when data is read from the memory chip.

Since Claim 25 of Appln. No. 9/911,635 and Claims 27-28 of the instant Application teach multichip modules it would have been obvious to one of ordinary skill in the art at the time the invention was made to mount a buffer and error correction code chips on each of the first and second modules of Claim 25, as recited in Claims 27-28, in order to apply the above-mentioned functions of buffers and ECC chips to the multichip modules and thereby enhance the performance and functionality of the claimed multichip module system of Claim 25 of Appln. 09/911,635.

9. This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Rejections Based On Prior Art

10. The following references were relied upon for the rejections hereinbelow:

Karabatsos (US 6,266,252 B1)* *Ilkbahar* (US 6,026,456)

Sanwo et al. (US 5,530,623)*

*Already made of record by Applicant's IDS, Paper No. 4.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

12. Claims 1-3, 12 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Ilkbahar.

As to Claim 1, Ilkbahar discloses, in Fig. 3: first and second modules 332 and 322 (each module comprising at least the following parts: *a substrate* with *signal lines* and having *at least one chip* mounted thereon; col.6: 31-32); a circuit board 300 including first and second module connectors 330 and 320 to receive first and second modules 332 and 322, respectively; a first path of conductors extending from the circuit board 300 (the first path beginning with bus lines 305) to the first module connector 330, to the first module 332, back to the first module connector 330, to the circuit board 300, to the second module connector 320, to the second module 322, and to on module terminations (i.e., on-chip terminations, the at least one chip 324 constituting *a part of the second module 322*, as indicated above; col.6: 35-36) of the second module; a second path of conductors extending from the circuit board 300 (the second path beginning with bus lines 305) to the second module connector 320, to the second module 322, back to the second module connector 320, to the circuit board 300, to the first module connector 330, to the first module 332, and to on module terminations (i.e., on-chip terminations, the at least one chip 334 constituting *a part of the first module 332*, as indicated above; col.6: 35-36) of the first module.

As to Claim 2, Ilkbahar further discloses, in Fig. 3: the first and second module connectors 330 and 320 each have front sides and back sides (respectively comprising

one of each of the pair of longer sides), and the first path extends from the back side of the first module 332 to the back side of the second module 322 (the module back sides are, arbitrarily, the faces of the modules not visible to the viewer; the front sides of the modules are the module faces visible to the viewer).

As to Claim 3, Ilkbahar further discloses, in Fig. 3: the first and second module connectors 330 and 320 have front sides and back sides (respectively comprising one of each of the pair of longer sides), and the first path extends from the back side of the first module 332 to the front side of the second module 322 (the module back sides are, arbitrarily, the faces of the modules not visible to the viewer; the front sides of the modules are the module faces visible to the viewer).

As to Claim 12, Ilkbahar further discloses, in Fig. 3, a controller 310 coupled to the first and second paths (col.6: 15-17).

As to Claim 13, Ilkbahar further discloses, in Fig. 3, circuit board 300 is a printed circuit board and a motherboard (col.6: 11-13).

13. Claims 16-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Sanwo et al.

As to Claim 16, Sanwo et al. discloses, in Figs. 1-3: a circuit board 15 including first and second module connectors 21 and 22 each including module slots; a first path of conductors 73 (consisting of segments 73A-H) extending from the circuit board 15 (segment 73A) to the first module connector 21 to a first group 61L of module connector contacts 61 of the first module connector 21, extending from a second group 61R of module connector contacts 61 of the first module connector 21 to circuit board 15

(segment 73B), to the second module connector 22, to a first group of module connector contacts 61L on the second module connector (col.3: 41-47), there being a gap between the first and second groups 61L and 61R of module connector contacts (Figs. 1 and 2; col.3: 3-8 and 59-62) of the first module connector 21; a second path of conductors (i.e., another of the plurality of transmission lines of which conductors 73 are representative; col.4: 7-10) extending from the circuit board 15 (specifically, the circuit board conductor segment analogous to segment 73C of the first path) to the second module connector 22 to a first group 61R of module connector contacts 61 of the second module connector 22, extending from a second group 61L of module connector contacts 61 of the second module connector 22 to circuit board 15 (specifically, the conductor segment analogous to segment 73B of the first path), to the first module connector 21, to a first group 61R of module connector contacts 61 on the first module connector 21, there being a gap between the first and second groups 61R and 61L of module connector contacts 61 (Figs. 1 and 2; col.3: 3-8 and 59-62) of the second module connector 22.

As to Claims 17 and 19 (as best understood by the Examiner in view of the 35 USC § 112, 2nd paragraph rejection, above), Sanwo et al. further discloses there are module connector connections between the circuit board 15 and the first and second module connectors 21 and 22 on the first path, and also on the second path (Fig. 2; col.3: 3-8).

As to Claim 18, Sanwo et al. further discloses that there are additional paths having a path like that of the first path and other additional paths having a path like that of the second path (col.4: 7-10).

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ilkbahar in view of Karabatsos.

I. Ilkbahar discloses that first and second modules 332 and 322 are connected to module connectors 330 and 320, respectively, but does not teach that first and second modules 332 and 322 and corresponding module connectors 330 and 320 are keyed so the first and second modules 332 and 322 each may be received in only one rotational orientation.

II. Karabatsos discloses modules 10, 12, 14 mounted in slots of connectors 8 wherein the modules 10, 12, 14 and the connectors 8 are keyed (note the notches separating portions of finger contacts 5 on module 10; Fig. 1) so that modules 10, 12, 14 can each be received in only one rotational orientation in the corresponding connectors 8 in order to ensure proper electrical connection of the modules 10, 12, 14 to the connectors 8 on motherboard 28.

III. Since both Ilkbahar and Karabatsos mount multichip memory modules to a motherboard, then it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the first and second modules of Ilkbahar with the keying structures taught by Karabatsos so that the modules of Ilkbahar may be received in the corresponding connector in only one rotational orientation in order to ensure proper electrical connection of the modules to the connectors on the motherboard in Ilkbahar, as taught by Karabatsos.

16. Claims 5, 7, 8 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ilkbahar.

As to Claim 5:

I. Ilkbahar discloses that the first and second modules 332 and 322 are can be added or removed without requiring system reconfiguration (col.6: 36-40) but does not teach that first and second modules 332 and 322 are interchangeable so that the first module 332 may be received by the second module connector 320 and the second module 322 may be received by the first module connector 330.

II. However, it would have been obvious to one of ordinary skill in the art to arrange the connectors 330 and 320 of Ilkbahar to receive the same type of modules, say, memory modules (col.4: 15-18), for enhancing memory capacity in a system, wherein the modules have the same chips, circuitry and keying, and thereby the first module may be inserted into the second connector and the second module may be inserted into the first connector with the same electronic and functional result as the first module inserted into the first connector and the second module inserted into the second

connector, thereby enhancing the memory capacity of the system regardless of which module was received by a particular connector, and since the keying would be the same, greatly facilitating the upgrading of memory by the user and preventing insertion error.

As to Claims 7 and 8:

I. Ilkbahar discloses that modules 332 and 322 can be multichip modules, memory modules, etc. (col.4: 15-18) but does not teach the specific circuitry and components mounted thereon, including buffers and error correction code chips, for an application.

II. Buffers and error correction code chips are old and well-known devices for performing specific functions in an electronic circuit mounted on a modular or system circuit board. Buffers have various electronic circuit functions; e.g., as storage sites that temporarily store data during data transfers to compensate for differences in data flow rates. Error correction code (ECC) chips are typically used for generating correction code when data is written into a memory chip and for checking "read" data to correct errors when data is read from the memory chip.

III. Since Ilkbahar discloses multichip modules including memory devices, then it would have been obvious to one of ordinary skill in the art at the time the invention was made to use buffers and ECC chips on the modules 332 and 322 of Ilkbahar in order to enable the disclosed electronic system by managing the data flow between the modules 332 and 322 and the memory chips thereon.

As to Claim 15:

I. Ilkbahar discloses a first path and a second path, as claimed in base Claim 1, wherein a portion of the path is on the first and second modules and 332 and 322 and includes chips 334 and 324 thereon, but does not teach additional paths like that of the first path and the second path.

II. Since Ilkbahar discloses that the first and second modules 332 and 322 are multichip modules (col.4: 11-18), and since the multichip modules may have a plurality of chips mounted thereon in any configuration suitable for an application, then it would have been obvious to one of ordinary skill in the art at the time the invention was made to have additional paths having a path like that of the first path coupling to additional chips 324 on the second module 322 and other additional paths having a path like that of the second path coupling to additional chips 334 of the first module 332 in order to increase the functionality or memory capacity of the electronic system as well as enhancing system performance while reducing system power consumption (col.7: 61-65 and col.8: 49-67).

17. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sanwo et al. in view of Karabatsos.

I. Sanwo et al. discloses that first and second modules 31 and 32 are connected to module connectors 21 and 22, respectively, but does not teach that first and second module connectors 21 and 22 are keyed such that a similarly keyed module (modules 31 and 32, respectively) can be inserted in only one orientation into the corresponding module slot.

II. Karabatsos discloses modules 10, 12, 14 mounted in slots of connectors 8 wherein the modules 10, 12, 14 and the connectors 8 are keyed (note the notches separating portions of finger contacts 5 on module 10; Fig. 1) so that modules 10, 12, 14 can each be received in only one rotational orientation in the corresponding connectors 8 in order to ensure proper electrical connection of the modules 10, 12, 14 to the connectors 8 on motherboard 28.

III. Since both Sanwo et al. and Karabatsos mount multichip memory modules to a motherboard, then it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the first and second modules and module connectors of Sanwo et al. with the keying structures taught by Karabatsos so that the modules of Sanwo et al. may be received in the corresponding connector in only one rotational orientation in order to ensure proper electrical connection of the modules to the module connectors on the circuit board in Sanwo et al., as taught by Karabatsos.

Allowable Subject Matter

18. Claims 23 and 24 have been allowed.

19. Claims 6, 9-11 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

20. The following is a statement of reasons for the indication of allowable subject matter:

As to Claim 6, patentability resides in the limitation wherein *each of the X paths couples to stubs for a different two of the 2X chips of the first module and for a different two of the 2X chips of the second module*, in combination with the other limitations of the claim.

As to Claim 9, patentability resides in the limitation wherein *the error correction code chips are terminated on the circuit board*, in combination with the other limitations of the claim.

As to Claim 10, patentability resides in **the combination** wherein: **1)** *a first section of the first path couples to stubs for only first and second chips of the first module, and a second section of the first path couples to stubs for only first and second chips of the second module*; **and 2)** *a first section of the second path couples to stubs for only third and fourth chips of the second module and a section of the second path couples to stubs for only third and fourth chips of the first module*, in combination with the other limitations of the claim.

As to Claim 11, patentability resides in **the combination** wherein: **1)** *a first section of the first path couples to stubs for only one chip of the first module, and a second section of the first path couples to stubs for only one chip of the second module*; **and 2)** *a first section of the second path couples to stubs for only one chip of the second module and a section of the second path couples to stubs for only one chip of the first module*, in combination with the other limitations of the claim.

As to Claim 14, patentability resides in the limitation wherein *impedances of the paths in the modules are at least 50% higher than the paths on the circuit boards*, in combination with the other limitations of the claim.

As to Claims 21-29 (subject to the Statutory Double Patenting rejection of Claims 21, 22 and 25-29, above), patentability resides in the limitation wherein *a first section of the second path, which is a short loop through section, couples to stubs for third and fourth chips of the second module and a section of second path couples to stubs for third and fourth chips of the first module*, in combination with the other limitations of base Claim 21.

21. As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Conclusion

22. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Osaka et al. (US 6,438,012 B1) discloses modules 2-2, 2-3 and 2-4 in connectors d2, d3 and d4 mounted on motherboard 1, and a first path 1-1 which includes a loop-through section which is, in turn, connected to memory chips 10-2 through 10-7 by stubs 1-2 through 1-7; the modules further include on-module terminations Rtt (Figs. 1 and 2).

Osaka et al. (US 5,638,402) discloses a stub as a portion of the bus connecting line 1-2 from an end (or a bending point) of the parallel coupling portion P to the semiconductor integrated circuit 10-2, provided for transferring a signal thereto (Fig. 1; col.5: 26-31).

Perino et al. (US 6,067,594) discloses that "a stub is defined as a length of line tapped from a transmission line and having a round trip delay which is greater than the rise time (or fall time) of the signal" (col.2: 5-8). Perino et al. also teaches a keyed module and corresponding keyed connector (Fig. 5; col.5: 14-17 and 58-65).

La Rue (US 6,081,430) discloses controlled impedance lines 13 that are called "loop-through" because "the transmission line starts on the mother board, connects to a transmission line on the daughter board and then connects back to the mother board" (col.3: 35-41). La Rue further discloses stubs 21 between the lines 13 and transceivers 7 (Fig. 4; col.3: 50-52).

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 703-308-1205. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on 703-305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7382 for regular communications and 703-308-7382 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

John B. Vigushin
Examiner
Art Unit 2827

jbv
December 13, 2002